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Appl. No. 10/826,038  
Reply to Office Action of March 18, 2008  
Amendment dated July 18, 2008

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A solid-state imaging device comprising:
  - unit pixels including: ~~as constituent elements~~
  - a charge generating section for generating a charge in an amount corresponding to a light received,
  - a charge storing part for storing a charge generated by the charge generating section,
  - a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,
  - a pixel signal generating section for generating a pixel signal ~~commensurate with~~ corresponding to the signal charge stored in the charge storing part, and
  - a reset section for resetting a level of ~~the signal charge at~~ the charge storing part;
  - a transfer line connected commonly with other unit pixels and connected to the transfer gate section;
  - a transfer drive buffer for driving the transfer line;

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a reset line connected commonly with other unit pixels and connected to the reset section;

a reset drive buffer for driving the reset line;

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section;

a drain drive buffer for driving the drain line; and

a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;

whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section ~~onto~~ to the signal line, is carried out under potential control at the charge storing part; and

wherein an off transition time, ~~on~~ of a voltage waveform on the drain line when ~~to be~~ driven by the drain drive buffer, ~~of~~ ~~upon applying a drive pulse to the drain drive buffer,~~ is five times or greater and ten thousand times or smaller relative to an off transition time on any of the signals applied to the reset line when ~~to be~~ driven by the reset drive buffer and the transfer line when ~~to be~~ driven by the transfer driven buffer.

2. (Currently Amended) A solid-state imaging device according to claim 1, wherein the off transition time ~~on~~ of the

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signal applied to the drain line is in a range of 50 to 600 times relative to an off transition time of a signal applied to the ~~on~~ ~~any of the reset line or~~ ~~and~~ the transfer line.

3. (Currently Amended) A solid-state imaging device according to claim 1, further comprising a pixel region arranged with the unit pixels in a two-dimensional matrix form, having ~~to~~ ~~have~~ a display resolution on the pixel region conforming to a VGA rating, wherein the off transition time of a signal applied to ~~on~~ the drain line is 10 nanoseconds or greater and 1000 nanoseconds or smaller.

4. (Currently Amended) A solid-state imaging device according to claim 3, wherein the off transition time of a signal applied to ~~on~~ the drain line is 40 nanoseconds or greater and 600 nanoseconds or smaller.

5. (Currently Amended) A solid-state imaging device according to claim 4, wherein the off transition time of a signal applied to ~~on~~ the drain line is 170 nanoseconds or greater.

6. (Currently Amended) A solid-state imaging device according to claim 1, wherein the off transition time of a signal applied to ~~on~~ the drain line is a half of a pixel clock period or greater and an off-period or smaller ~~to the drain line~~.

7. (Original) A solid-state imaging device according to claim 1, wherein the transfer drive buffer includes a transistor

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connected at least to the transfer line, the reset drive buffer includes a transistor connected at least to the reset line, and the drain drive buffer includes a transistor connected at least to the drain line, wherein the transistor connected to the drain line has a W/L ratio (W is a gate width, L is a gate length) set in a range of 1/5 times to 1/2500 times greater than any of a W/L ratio of the transistor connected to the transfer line and a W/L ratio of the transistor connected to the reset line.

8. (Original) A solid-state imaging device according to claim 7, wherein the transistor connected to the drain line has a W/L ratio set in a range of 1/10 times to 1/500 times greater than any of a W/L ratio of the transistor connected to the transfer line and a W/L ratio of the transistor connected to the reset line.

9. (Currently Amended) A solid-state imaging device according to claim 1, further comprising a resistance element for limiting a drive current provided between an off-side reference line of the drain drive buffer and a reference power source ~~regulating an off voltage to the drain line.~~

10. (Currently Amended) A solid-state imaging device according to claim 1, further comprising a current source for regulating a drive current provided between an off-side reference

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line of the drain drive buffer and a reference power source  
~~regulating an off voltage to the drain line.~~

Claims 11.-18. (Canceled)

19. (Currently Amended) A solid-state imaging device  
comprising:

unit pixels including: ~~as constituent elements~~

a charge generating section for generating a signal charge in  
an amount corresponding to a light received,

a charge storing part for storing a charge generated by the  
charge generating section,

a transfer gate section arranged between the charge  
generating section and the charge storing part and for  
transferring the signal charge generated by the charge generating  
section ~~to the charge storing part,~~

a pixel signal generating section for generating a pixel  
signal ~~commensurate with~~ corresponding to the signal charge stored  
~~at~~ in the charge storing part, and

a reset section for resetting the signal charge ~~at~~ stored in  
the charge storing part;

a transfer line connected commonly with other unit pixels and  
connected to the transfer gate section;

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a transfer drive buffer for driving the transfer line;  
a reset line connected commonly with other unit pixels and connected to the reset section;  
a reset drive buffer for driving the reset line;  
a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section;  
a drain drive buffer for driving the drain line; and  
a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;  
~~whereby a pixel select operation, for~~ wherein outputting the pixel signal generated by the pixel signal generating section ~~onto~~ to the signal line, ~~is~~ carried out under potential control at the charge storing part; and  
wherein an off transition time, ~~on~~ of a voltage waveform applied to ~~on~~ the drain line ~~to be~~ when driven by the drain drive buffer ~~of upon applying a drive pulse to the drain drive buffer,~~ is ~~given~~ longer than an off transition time on any of the reset line when ~~to be~~ driven by the reset drive buffer and the transfer line when ~~to be~~ driven by the transfer driven buffer.

20. (Currently Amended) A solid-state imaging device comprising:

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a solid-state imaging element having

unit pixels including: ~~as constituent elements,~~

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part ~~and~~ for transferring the signal charge generated by the charge generating section ~~to the charge storing part,~~

a pixel signal generating section for generating a pixel signal corresponding to ~~commensurate with~~ the signal charge stored in ~~at~~ the charge storing part, and

a reset section for resetting the signal charge ~~at~~ stored in the charge storing part;

a transfer line connected commonly with other unit pixels and connected to the transfer gate section;

a reset line connected commonly with other unit pixels and connected to the reset section;

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section; and

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a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;

whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section ~~onto~~ to the signal line, is carried out under potential control at the charge storing part; and

a waveform shaping section for receiving a drive pulse for driving the drain line and carrying out a waveform shaping such that an off transition time, ~~on~~ for a voltage waveform applied to ~~in-driving~~ the drain line, is given longer than an off transition time ~~on~~ of a voltage waveform applied to ~~in-driving any of the~~ reset line and the transfer line.

21. (Currently Amended) A solid-state imaging device according to claim 20, wherein the waveform shaping section carries out a waveform shaping such that an off transition time for ~~on~~ a voltage waveform applied to ~~in-driving~~ the drain line is five times or greater and ten thousand times or smaller than the off transition time for signals applied to ~~on both~~ the reset line and the transfer line.

22. (Currently Amended) A drive control method for a solid-state imaging device comprising:

unit pixels including: ~~as constituent elements,~~



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a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge signal generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal ~~commensurate with~~ corresponding to the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge ~~at~~ stored in the charge storing part[,];

a transfer line connected commonly with other unit pixels and connected to the transfer gate section;

a reset line connected commonly with other unit pixels and connected to the reset section[,];

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section[,]; and

a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels,;

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whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section ~~onto~~ to the signal line, is carried out under potential control at the charge storing part, the drive control method characterized in that:

the drain line is driven such that an off transition time, ~~on a voltage waveform in driving applied to~~ the drain line, is given longer than an off transition time of a ~~on a voltage waveform in driving applied to~~ any of the reset line and the transfer line.

23. (Currently Amended) A drive control method according to claim 22, wherein the drain line is driven such that an off transition time of ~~on a voltage waveform applied to in driving~~ the drain line is five times or greater and ten thousand times or smaller than the off transition time on both the reset line and the transfer line.

24. (Currently Amended) A solid-state imaging device comprising:

an imaging region arranged with a plurality of pixels; and  
a circuit region for supplying a drive pulse to the imaging region;

the pixel having :

a photoelectric converting section for generating a charge ~~commensurate with~~ corresponding to an amount of incident light,

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a charge storing part for storing a charge read from the photoelectric converting section ~~by a transfer gate section~~, and a reset section for resetting the charge stored at the charge storing part;

wherein the transfer gate is connected with a transfer line, the reset section is connected with a reset line, and the charge storing part is connected with a drain line ~~through the reset section~~;

the circuit region supplying a first pulse to ~~toward~~ the drain line, a second pulse to ~~toward~~ the reset line, and a third pulse to ~~toward~~ the transfer line;

the first pulse having a waveform longer in off transition time than a waveform of the second pulse and third pulse.